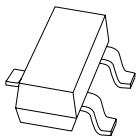


# BSS84

## P-channel enhancement mode vertical D-MOS transistor

Rev. 04 — 17 July 2007 Product data sheet

## 1. Product profile

### 1.1 General description

P-channel enhancement mode vertical D-MOS transistor in a SOT23 Surface-Mount Device (SMD) package.

### 1.2 Features

- Low threshold voltage
- High-speed switching
- Direct interface to CMOS and Transistor-Transistor Logic (TTL)
- No secondary breakdown

### 1.3 Applications

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers

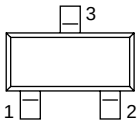
### 1.4 Quick reference data

- $V_{DS} \leq -50$ V
- $R_{DSon} \leq 10\ \Omega$
- $I_D \leq -130$ mA
- $P_{tot} \leq 250$ mW

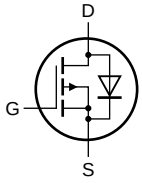
## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | gate (G) | | |
| 2 | source (S) | | |
| 3 | drain (D) | | |




**SOT23 (TO-236AB)**




*001aaa025*

## 3. Ordering information

**Table 2. Ordering information**

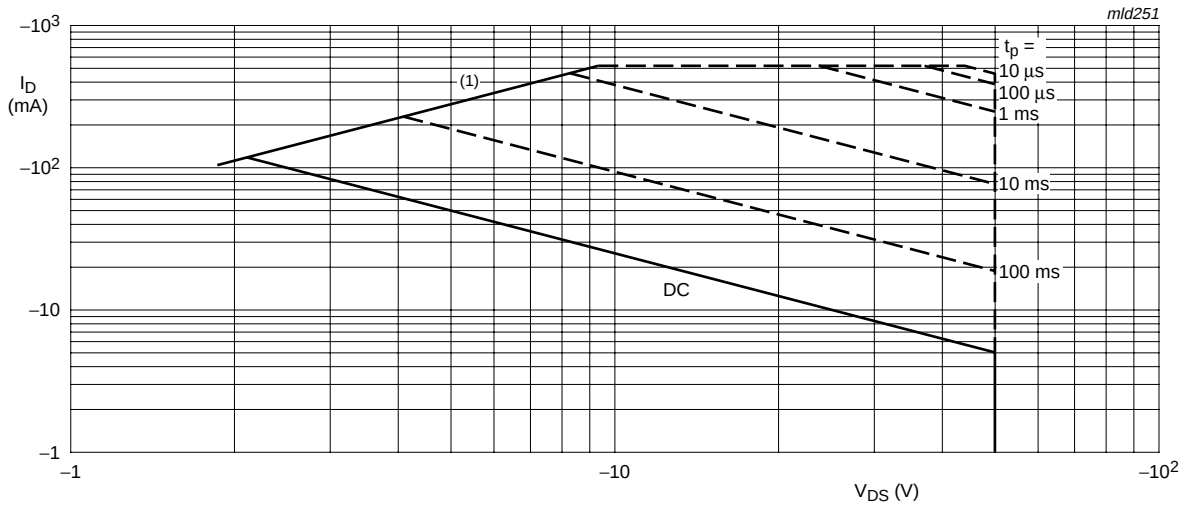
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BSS84 | TO-236AB | plastic surface-mounted package; 3 leads | SOT23 |

## 4. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | - | –50 | V |
| $V_{GS}$ | gate-source voltage | | - | ±20 | V |
| $I_D$ | drain current | $T_{sp}$ = 25 °C; $V_{GS}$ = –10 V; see Figure 1 | - | –130 | mA |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = –10 V | - | –75 | mA |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; see Figure 1 | - | –520 | mA |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; see Figure 4 | - | 250 | mW |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | | –65 | +150 | °C |




$T_{sp}$ = 25 °C

(1) $R_{DSon}$ limitation

**Fig 1. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

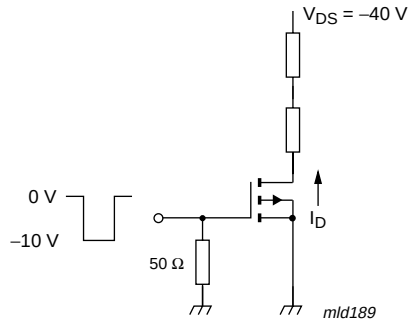



Fig 2. Switching time test circuit

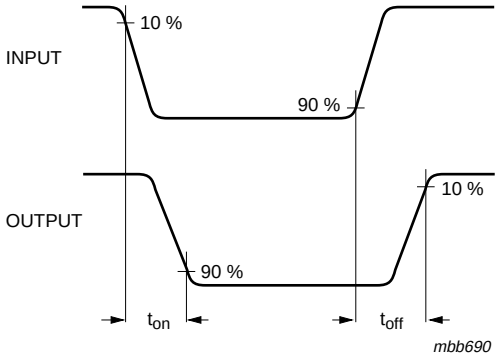



Fig 3. Input and output waveforms

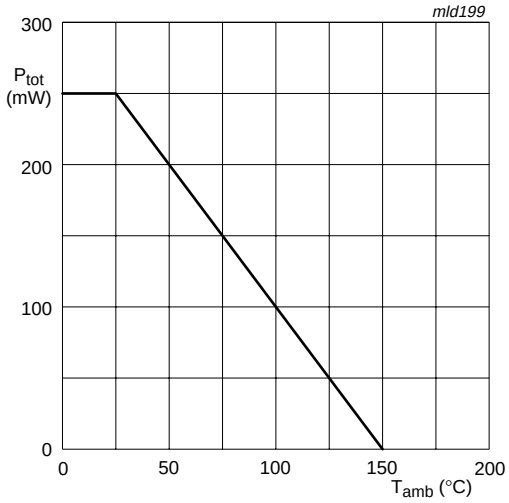



Fig 4. Power derating curve

## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | see Figure 5 | [1] | - | - | 500 | K/W |

[1] Mounted on a printed-circuit board; vertical in still air

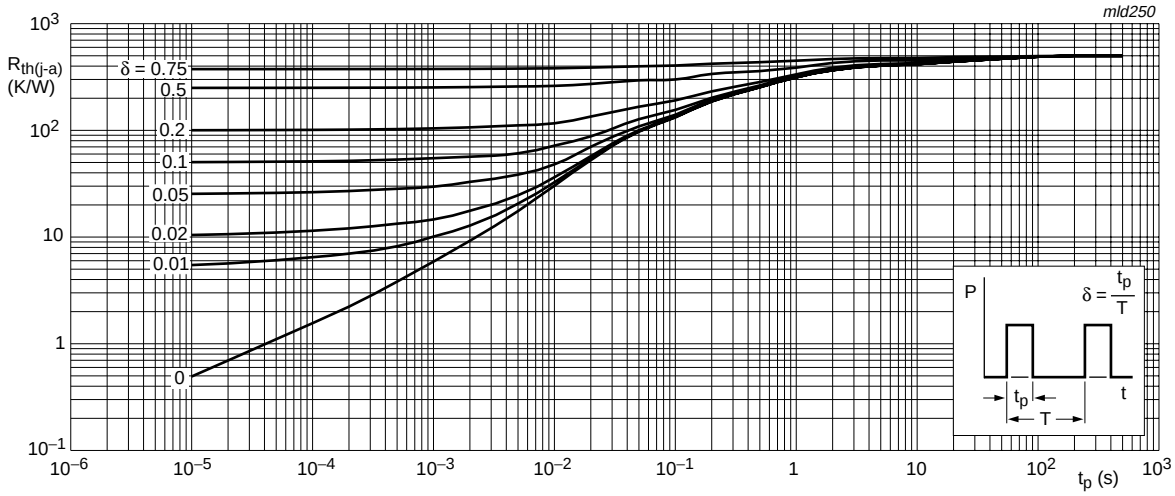


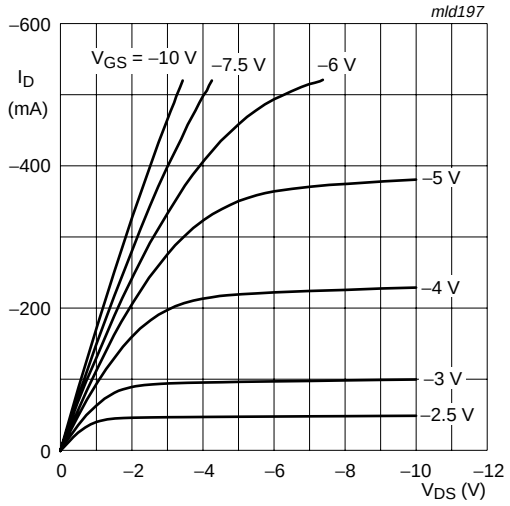

**Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration**

## 6. Characteristics

**Table 5. Characteristics**

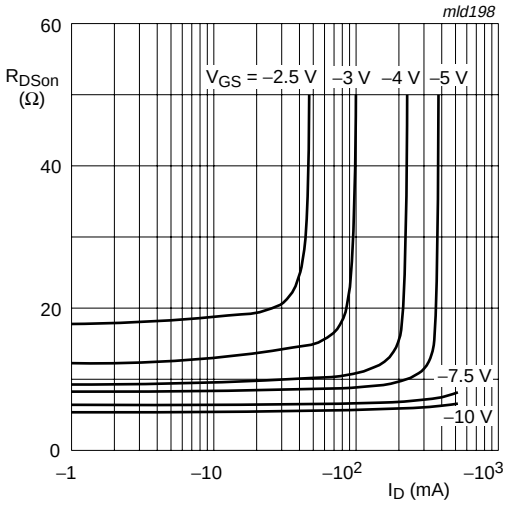
*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = –10 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | –50 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = –1 mA; $V_{DS}$ = $V_{GS}$; see Figure 10 | | | | |
| | | $T_j$ = 25 °C | –0.8 | - | –2 | V |
| | | $T_j$ = –55 °C | - | - | –1.8 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = –40 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | –100 | nA |
| | | $V_{DS}$ = –50 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | –10 | µA |
| | | $T_j$ = 125 °C | - | - | –60 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | - | - | ±100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = –10 V; $I_D$ = –130 mA; see Figure 7 and 9 | | | | |
| | | $T_j$ = 25 °C | - | 6 | 10 | Ω |
| **Dynamic characteristics** | | | | | | |
| $\|Y_{fs}\|$ | transfer admittance | $V_{DS}$ = –25 V; $I_D$ = –130 mA | 50 | - | - | mS |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = –25 V; f = 1 MHz; see Figure 11 | - | 25 | 45 | pF |
| $C_{oss}$ | output capacitance | | - | 15 | 25 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 3.5 | 12 | pF |
| $t_{on}$ | turn-on time | $V_{DS}$ = –40 V; $V_{GS}$ = 0 V to –10 V; $I_D$ = –200 mA; see Figure 2 and 3 | - | 3 | - | ns |
| $t_{off}$ | turn-off time | $V_{DS}$ = –40 V; $V_{GS}$ = –10 V to 0 V; $I_D$ = –200 mA; see Figure 2 and 3 | - | 7 | - | ns |



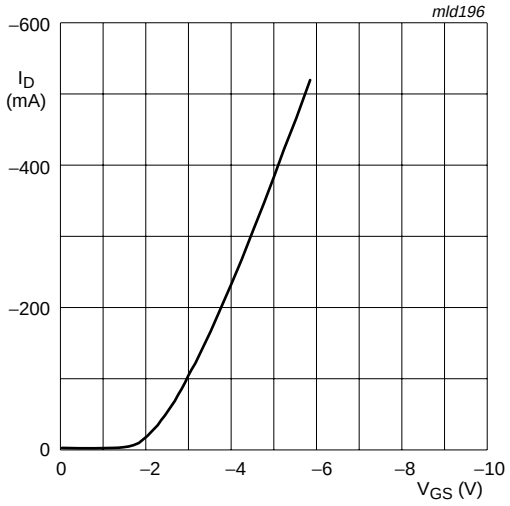

$T_j$ = 25 °C

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



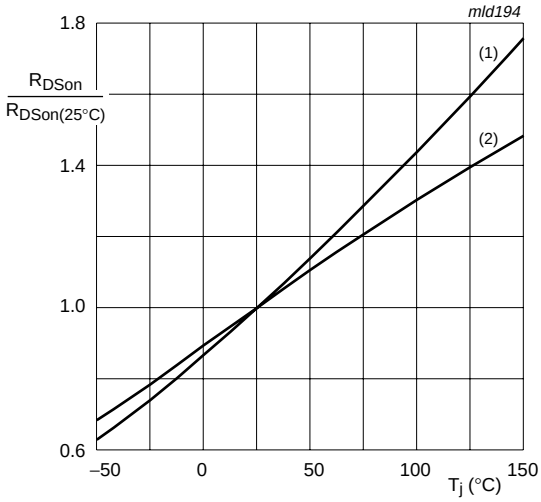

$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**




$T_j$ = 25 °C; $V_{DS}$ = −10 V

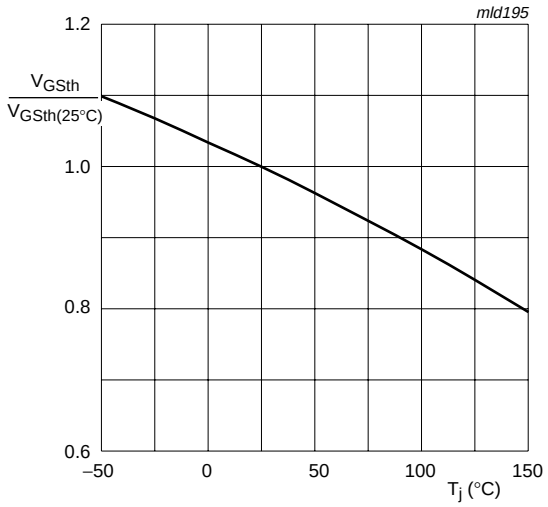
**Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values**




(1) $I_D$ = −130 mA; $V_{GS}$ = −10 V

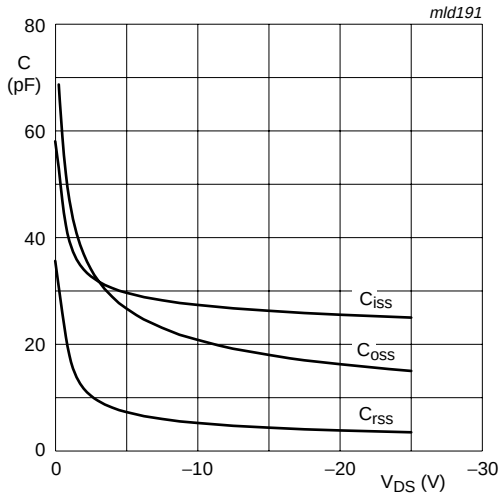
(2) $I_D$ = −20 mA; $V_{GS}$ = −2.4 V

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature**




$I_D$ = –1 mA; $V_{DS}$ = $V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**

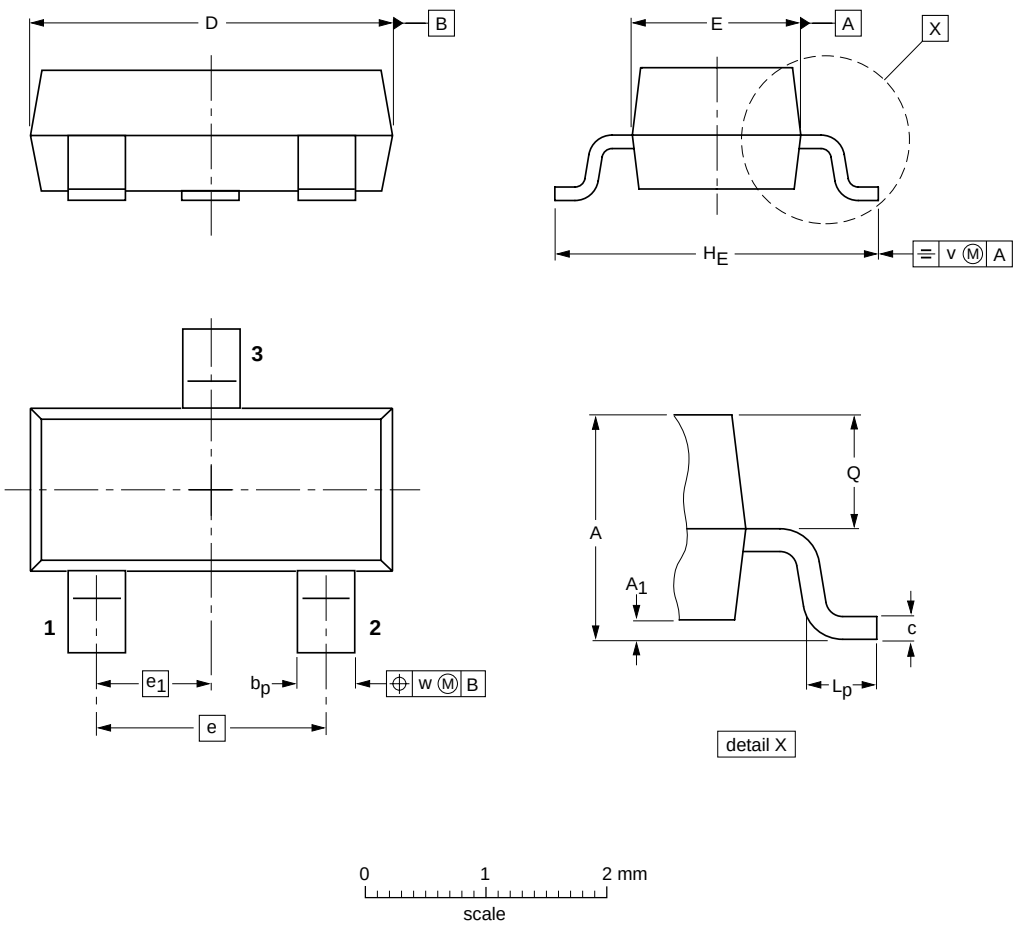



$V_{GS}$ = 0 V; f = 1 MHz

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

## 7. Package outline

**Plastic surface-mounted package; 3 leads** **SOT23**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max. | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1 | 0.48<br>0.38 | 0.15<br>0.09 | 3.0<br>2.8 | 1.4<br>1.2 | 1.9 | 0.95 | 2.5<br>2.1 | 0.45<br>0.15 | 0.55<br>0.45 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT23 | | TO-236AB | | | | ~~04-11-04~~<br>06-03-16 |

**Fig 12. Package outline SOT23 (TO-236AB)**

## 8. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BSS84_4 | 20070717 | Product data sheet | - | BSS84_3 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Marking code has been removed. | | | |
| BSS84_3<br>(9397 750 11693) | 20030804 | Product specification | - | BSS84_2 |
| BSS84_2<br>(9397 750 02333) | 19970618 | Product specification | - | BSS84_1 |
| BSS84_1 | 19950407 | Product specification | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Document identifier: BSS84_4